Office Action Summary	Application No.	Applicant(s)	
	10/676,758	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Jonathan R. Plante	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :01 October 2003, 20 February 2004, 23 April 2004, 20 July 2005, and 19 October 2007.

DETAILED ACTION

1. The instant application having Application Number: 10/676,758 filed on 01 October 2003 has a total of 32 claims pending in the application; there are 3 independent claims and 29 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 01 October 2003, 20 February 2004, 23 April 2004, 20 July 2005, and 19 October 2007 have been received. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the Examiner.

Specification

4. The disclosure is objected to because of the following informalities:

   a. (Page 10, Line 10): Correct "the local bus 10" to be either "host bridge (Figure 1B, 10)" or "PCI-X BUS (Figure 1A, 6).

b. Please correct specification to be consistent with the term "the system memory" or "host memory" in respect to (Figure 2, 128). Maintain term consistence throughout specification.

c. (Page 22, Line 24): Replace "The system 130" with "The descriptor management unit 130" to coincide with Figure 2.

d. (Page 29, Line 22): Replace "IPsec processor 150" with "IPsec processor 148" to coincide with Figure 2.

e. (Page 29, Line 26): Replace "IPsec processor 150" with "IPsec processor 148" to coincide with Figure 2.

f. (Page 31, Line 14): Replace "network port manager 175" with "network port manager 182" to coincide with Figure 3.

g. (Page 31, Line 21): Replace "power management unit 188" with "power management unit 175" to coincide with Figure 3.

h. (Page 31, Line 24): Replace "power management unit 188" with "power management unit 175" to coincide with Figure 3.

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

   a. (Figure 1C, 40)

   b. (Figure 1D, 58)

7. The drawings are objected to because:

   a. (Figure 1E, 130): Replace "DMU" with "Descriptor management unit" for clarity.

   b. (Figure 2, 124): Increase the boldness of the line indicating unit 124 to clarify what unit 124 contains.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be

notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Claims 2, 16, 19, 22, 28, and 31 are objected to because of the following informalities:

a. (Claim 2, Line 3): Replace “a lower limit” with “the lower limit” to resolve potential lack of antecedent basis issues.

b. (Claim 2, Line 3): Replace “a number” with “the number” to resolve potential lack of antecedent basis issues.

c. (Claim 2, Lines7): (Claim, Line): Replace “a full cache” with “the full cache” to resolve potential lack of antecedent basis issues.

d. (Claim 16, Line 4): Replace “a full cache” with “the full cache” to resolve potential lack of antecedent basis issues.

e. (Claim 19, Line 2): Replace “the sum” with “a sum” to resolve potential lack of antecedent basis issues.

f. (Claim 19, Line 2): Replace “the number” (appears twice) with “a number” to resolve potential lack of antecedent basis issues.

g. (Claim 22, Line 3): Replace “a lower” with “the lower” to resolve potential lack of antecedent basis issues.

h. (Claim 22, Line 6): Replace “a full cache” with “the full cache” to resolve potential lack of antecedent basis issues.

i. (Claim 28, Line 2): Replace “the difference” with “a difference” to resolve potential lack of antecedent basis issues.

j. (Claim 31, Line 4): Replace “a full cache” with “the full cache” to resolve potential lack of antecedent basis issues.

k. (Claim 31, Line 5): Replace “a first with “the first” to resolve potential lack of antecedent basis issues.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

(Claims 1, 15, 20, and 21): Recite the limitations of writing data from a peripheral device using a full cache line write (writing data to a cache). The specification fails to disclose to one skilled in the art how a peripheral device can access and write data to a cache.

(Claims 2-19, 22-32): Are rejected for incorporating the defects of the Claims from which they depend.

Appropriate correction is required.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(Claims 1, 20, and 21): The terms "a lower limit" and “a first value” in Claims 1, 20, and 21 are relative terms which renders the claims indefinite. The term "a lower limit" and “a first value” is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

(Claims 1, 2, 15, 16, 20, 21, 22, and 31): Recite the limitation of “transferring a current data entry to the host system memory using a full cache line write” (Claim 1, Line 5), (Claim 2, Line 7), (Claim 16, Line 4), (Claim 20, Line 6), (Claim 21, Line 5), (Claim 22, Line 6), (Claim 31, Line 3) and also in Claim 15 recites the limitation “a partial cache line write” (Claim 15, Line 2). The usage of the term “cache line” is in conflict with the claims

language in respect to system memory. The term system memory in the art commonly refers to primary memory (i.e. SRAM, DRAM, SDRAM, volatile memory, etc) and secondary memory (i.e. hard disk drives, tape drives, optical drives, and non-volatile memory) where these memories have a recognized structure and are address based in accessing. A cache memory (i.e. 1st level cache, 2nd level cache) associated with a processor is a specialized type of memory that is structurally designed and accessed differently then system memory. As a result the Claim language is indefinite and ambiguous.

The Examiner further notes that cache line data sizes are in the range of bits 32 bits to 128 bits, while the data being transferred by descriptors are in multiple bytes, mega-bytes, gigabytes based on the amount of data to be transferred.

The Examiner will interpret the full cache line as referring to writing the full amount of data to the data queue in the system memory if there is enough available space.

(Claims 3-19, 22-32): Are rejected for incorporating the defects of the Claims from which they depend.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **As far as Examiner can interpret the Claims in view of 35 USC 112 rejections set forth above, Claims 1, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al. (US 6,212,593 B1 April 3, 2001).**

(Claims 1, 20, and 21): Pham et al. teaches: "A method for transferring data entries from a peripheral to a data queue in a host system memory, **[Figure 2 depicts a DMA unit using a buffer descriptor ring (Figure 4, 300) for transferring data between peripheral device (Figure 2, Index 164, 148, 146) and system memory (Figure 2, 178) where system memory contains transmit and receive buffers (Figure 3, Index 206a, 206b, 206c)]** the method comprising: determining a lower limit on a number of available data entry positions in the data queue; **[The transmitting channel of the Smart DMA reads the length (equated to available data entry positions) of the corresponding buffer (equated to data queue (Figure 3, 206a-c)) by reading the BCNT (254) (byte count value) (C 1, L 42-46) where the BCNT is the size of the receive buffer (C 8, L 30)]** and selectively transferring a current data entry to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value" **[When the start of packet value (STP) value (258) and end of packet**

(ENP) value (260) are set the packets (equated to current data) fin into a single buffer (206) (C 7, L 64-65). Further Figure 7 depicts in Box 406 the terminal count (TC) being greater then zero data being transmitted to the buffer and when TC is equal to zero and the end of packet value is 1 that all data has been transferred to the buffer and the transfer is complete resulting in a full transfer of data to the data queue in the memory). Additionally the current data length can be less then the buffer byte count BCNT of the receiving buffer (C 8, L 18-20)]

(Claim 20): Pham et al. teaches: "A system for transferring incoming data status entries from a peripheral to a host system memory, comprising: a descriptor management system in the peripheral, **[Figure 2 depicts a DMA unit using a buffer descriptor ring (Figure 4, 300) for transferring data between peripheral device (Figure 2, Index 164, 148, 146) and system memory (Figure 2, 178) where system memory contains transmit and receive buffers (Figure 3, Index 206a, 206b, 206c)]** the descriptor management system adapted to determine a lower limit on a number of available incoming data status entry positions in an incoming data status ring in the host system memory, **[The transmitting channel of the Smart DMA reads the length (equated to available data entry positions) of the corresponding buffer (equated to data queue (Figure 3, 206a-c)) by reading the BCNT (254) (byte count value) (C 1, L 42-46) where the BCNT is the size of the receive buffer (C 8, L 30)]** and to selectively transfer a current incoming data status entry to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value" **[When the**

start of packet value (STP) value (258) and end of packet (ENP) value (260) are set the packets (equated to current data) fin into a single buffer (206) (C 7, L 64-65). Further Figure 7 depicts in Box 406 the terminal count (TC) being greater then zero data being transmitted to the buffer and when TC is equal to zero and the end of packet value is 1 that all data has been transferred to the buffer and the transfer is complete resulting in a full transfer of data to the data queue in the memory). Additionally the current data length can be less then the buffer byte count BCNT of the receiving buffer (C 8, L 18-20)].

(Claim 21): Pham et al. teaches: "A peripheral system for providing an interface between a host computer and an external device or network, the peripheral system comprising: a descriptor management system **[Figure 2 depicts a DMA unit using a buffer descriptor ring (Figure 4, 300) for transferring data between peripheral device (Figure 2, Index 164, 148, 146) and system memory (Figure 2, 178) where system memory contains transmit and receive buffers (Figure 3, Index 206a, 206b, 206c)]** adapted to determine a lower limit on a number of available data entry positions in a data queue in a host system memory, and to selectively transfer a current data entry to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value." **[The transmitting channel of the Smart DMA reads the length (equated to available data entry positions) of the corresponding buffer (equated to data queue (Figure 3, 206a-c)) by reading the BCNT (254) (byte count value) (C 1, L 42-46) where the BCNT is the size of the receive buffer (C 8, L 30)**

When the start of packet value (STP) value (258) and end of packet (ENP) value (260) are set the packets (equated to current data) fin into a single buffer (206) (C 7, L 64-65). Further Figure 7 depicts in Box 406 the terminal count (TC) being greater then zero data being transmitted to the buffer and when TC is equal to zero and the end of packet value is 1 that all data has been transferred to the buffer and the transfer is complete resulting in a full transfer of data to the data queue in the memory). Additionally the current data length can be less then the buffer byte count BCNT of the receiving buffer (C 8, L 18-20)].

15. **Claims 2-19 and 22-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al. (US 6,212,593 B1 April 3, 2001), and in further view of Garrett et al. (US 6,334,162 B1 December 25, 2001).**

(Claims 2-3, 22): In further view of Claims 1 and 21, Pham et al. teaches:

a. The application of the data queue being a circular buffer of descriptors in the system memory (C 1, L 44-50).
b. Figure 4, depicts a 4-entry Descriptor Ring (Figure 4, 302) in the system memory (Figure 4, 178).
c. The transmit ring count (Figure 3, 202) is used to count the number of buffer descriptors with the buffer descriptor ring (Figure 3, 204).
d. Figure 8, depicts a chain of descriptors being linked together and transferred allowing for the burst transfer of descriptors.

e. A transmit buffer descriptor (Figure 5A, 208) contains status and configuration data of the buffer descriptor (C 7, L 41-44).

Pham et al. teaches the application of overflow, underflow, and other errors associated with the descriptor buffers, in addition to the linking a chain of descriptors that are processed without interruption.

However Pham et al. fails to explicitly teach the data queue being an incoming status ring.

Garret et al. teaches:

a. A status queue (Figure 2, 23).
b. Burst processing of descriptors (C 3, L 65-67)

It would have been obvious to one skilled in the art to combine Pham et al. with Garret et al. to determine a lower limit on the number of available incoming data status entry positions in order to avoid the error condition of an under run situation where the descriptor ring reads erroneous data when over running valid descriptors in the descriptor ring.

(Claim 3): In further view of Claims 2, "wherein the lower limit is determined at least in part according to a number of unused incoming data descriptors" **[The transmit ring**

count (Figure 3, 202) is used to count the number of buffer descriptors with the buffer descriptor ring (Figure 3, 204).].

(Claim 4): In further view of Claims 3, Pham et al. teaches: "wherein the lower limit is determined at least in part according to a number of unused incoming data status entry positions remaining for a current incoming data descriptor" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 5): In further view of Claims 4, Pham et al. teaches: "wherein the lower limit is determined at least in part according to a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 6): In further view of Claims 5, Pham et al. teaches: "wherein determining the lower limit comprises calculating a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor minus 1." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 7): In further view of Claims 6, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line. **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 8): In further view of Claims 7, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entry positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 9): In further view of Claims 7, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 10): In further view of Claims 3, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entries positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 11): In further view of Claims 3, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 12): In further view of Claims 3, Pham et al. teaches: "wherein the number of unused incoming data descriptors is the difference between an incoming data status pointer and an incoming data descriptor write pointer." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 13): In further view of Claims 2, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entries positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 14): In further view of Claims 2, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claims 15 and 23): In further view of Claims 2 and 22, Pham et al. teaches:

a. "selectively transferring the current incoming data status entry to the host system memory using a partial cache line write if the lower limit is less than the first value" **[Depicted in Figure 6 box 406 the transfer of data continues unit the TC = 0 and ENP = 0 meaning all data has been transferred to the buffer].**

(Claim 31): In further view of Claims 2 and 22, Pham et al. teaches:

a. The application of chain descriptors together and chaining buffers together when the amount of data to be transferred exceeds the size of a buffer, the Smart DMA will use multiple buffers for the transfer of data (C 7, L 55-61).

(Claim 16): Is rejected for the same reasons as Claim 31 above since Claim 16 is broader then Claim 31.

(Claim 17): In further view of Claims 16, Pham et al. teaches: "wherein the first value is a number of unused incoming data status entries positions remaining in the current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 18): In further view of Claims 16, Pham et al. teaches: "wherein the first value is a number of incoming data status entries per cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 19): In further view of Claims 16, Pham et al. teaches: "wherein determining the lower limit comprises calculating the sum of the number of Unused incoming data descriptors and the number of unused incoming data status entry positions remaining for a current incoming data descriptor minus 1" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 24): In further view of Claims 22, Pham et al. teaches: "wherein the descriptor management system determines the lower limit at least in part according to a number of unused incoming data descriptors. **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 25): In further view of Claims 24, Pham et al. teaches: "wherein the descriptor management system determines the lower limit at least in part according to a number of unused incoming data status entry positions remaining for a current incoming data descriptor. **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 26): In further view of Claims 25, Pham et al. teaches: "wherein the descriptor management system determines the lower limit at least in part according to a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 27): In further view of Claims 26, Pham et al. teaches: "wherein the descriptor management system determines the lower limit as a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor minus 1." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 28): In further view of Claims 27, Pham et al. teaches: "wherein the descriptor management system determines the number of unused incoming data descriptors as the difference between an incoming data status pointer and an incoming data descriptor write pointer." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 29): In further view of Claims 22, Pham et al. teaches: wherein the first value is a number of unused incoming data status entry positions remaining in a current cache line." **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 30): In further view of Claims 22, Pham et al. teaches: wherein the first value is a number of incoming data status entries per cache line" **[(C 1-2, L 65-20), (C 8, L 18-20)].**

(Claim 32): In further view of Claim 22, Pham et al. teaches:

a. Local Area Network Controller (C 1, L 56).

Conclusion

16. In order to facilitate the prosecution of this Application the Examiner recommends that Applicant schedule an interview to clarify the invention in respect to the 35 USC 112 rejections and the claim language.

17. The Examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application. **Failure to show support can result in a non-compliant response.**

When responding to this office action, Applicant is advised that if Applicant traverses an obviousness rejection under 35 U.S.C. 103, a reasoned statement must be included

explaining why the Applicant believes the Office has erred substantively as to the factual findings or the conclusion of obviousness See 37 CFR 1.111(b).

18. Additionally Applicant is further advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday -- Thursday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jonathan R Plante/
Examiner, Art Unit 2182

/Tonia LM Dollinger/
Primary Examiner, Art Unit 2181